# Simple and Accurate Technique for Extracting the Parasitic Resistances of the Dual-Gate GaAs MESFET

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***Abstract*—A procedure to extract the extrinsic resistances of the dual-gate GaAs MESFET (DGFET) is described. Six dc measurement setups are used to generate nine independent relations from which all the unknown extrinsic resistances of the DGFET are extracted. The described technique distinguishes between the forward bias and the nonforward bias values of the channel resistance. The extrinsic resistances of 29 devices with different topologies are determined using the developed technique. The extracted resistances follow normal scaling rules versus gate width. The developed procedure is a practical and accurate approach to extract the extrinsic resistances of the DGFET.**

***Index Terms*—Dual-gate MESFET, equivalent circuit, parameters extraction.**

## I. Introduction

THE extrinsic resistances of the dual-gate GaAs MESFET (DGFET) are key parameters that affect the gain and the noise figure of the transistor. While several techniques for extracting the parasitic resistances of the single-gate FET have been reported [1]–[5], much less has been published to extract the extrinsic resistances of the DGFET [6]–[9]. The reported techniques make use of either dc or $S$-parameter measurements from which some relations between the unknown resistances are derived.

Applying the technique introduced by Dambrine *et al.* [4] to calculate the extrinsic resistances for a single-gate FET using $S$-parameter measurements, only five independent equations can be derived for the DGFET. Assuming common source connection, these equations are (port 1 is gate$_1$, port 2 is gate$_2$, and port 3 is the drain)

$$Re\,Z_{11} = R_{g1} + \frac{n_1 V_T}{I_{g1}} + \frac{R_{c1}}{3} + R_s \quad (1)$$

$$Re\,Z_{22} = R_{g2} + \frac{n_2 V_T}{I_{g2}} + \frac{R_{c2}}{3} + R_{12} + R_{c1} + R_s \quad (2)$$

$$Re\,Z_{33} = R_d + R_{c2} + R_{12} + R_{c1} + R_s \quad (3)$$

$$Re\,Z_{12} = Re\,Z_{13} = Re\,Z_{21} = Re\,Z_{31} = \frac{R_{c1}}{2} + R_s \quad (4)$$

$$Re\,Z_{23} = Re\,Z_{32} = \frac{R_{c2}}{2} + R_{12} + R_{c1} + R_s \quad (5)$$

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where $R_{g1}$, $R_{g2}$, $R_{c1}$, $R_{c2}$, $R_{12}$, $R_s$, and $R_d$ are the resistances of gate$_1$, gate$_2$, channel$_1$, channel$_2$, inter-gate, the source, and the drain, respectively; $n_1$ and $n_2$ are the ideality factors of gate$_1$ and gate$_2$ Schottky barriers, respectively; $V_T$ is the thermal voltage; $I_{g1}$ and $I_{g2}$ are the forward currents for gate$_1$ and gate$_2$, respectively.

Since there are seven unknown resistances to be extracted, two additional equations are required. Langrez *et al.* [6], [7] assumed that the channel resistances are equal (which is not valid for nonsymmetric devices) to reduce the number of unknowns. Even with this assumption, an additional equation is still required. Langrez *et al.* [6], [7] did not show how they extracted the six unknown resistances by using only five independent equations.

Tsironis and Meierer [8] introduced dc measurements to extract the extrinsic resistances of the DGFET. When extracting $R_s$, $R_d$, and $R_{12}$, the channel resistances were ignored. This assumption introduced a large error to the calculated extrinsic resistances since the channel resistances can be in the order of (or even larger than) $R_s$, $R_d$, or $R_{12}$.

To extract the extrinsic resistances of the DGFET, Deng and Chu[9] used the end-resistance method [10] to derive five independent equations and proposed to use other techniques to derive two additional independent equations. Using different techniques makes the extraction procedure complex. Furthermore, two of the five equations derived from the end-resistance technique are based on measurements performed when the source is floating. These measurements cannot be obtained for on-wafer devices that have sources grounded. Another drawback of the reported technique in [9] is that the forward bias and the nonforward bias values of the channel resistance are assumed to be equal.

In this paper, we introduce simple, yet accurate, dc measurements that generate nine independent equations to be used to determine the seven parasitic resistances of the DGFET. Each channel resistance is allowed to have two different values with and without forward bias applied to its controlling gate, resulting in nine unknowns. All the measurements are performed when the source is grounded which make this technique suitable for modeling on-wafer DGFETs whose sources are grounded.

## II. Extraction Procedure

The basic model of a DGFET is a cascode connection of two single-gate MESFETs $FET_1$ and $FET_2$ [11]. The dc equiv-

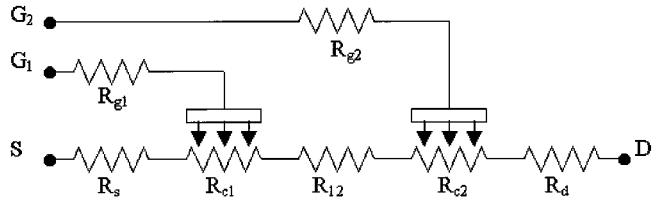


Fig. 1. DC equivalent circuit of cold DGFET with both gates forward biased [9].

alent circuit of the cold DGFET when both gates are forward biased is shown in Fig. 1. [9].

Using six different dc measurements, nine independent relations between the nine unknown resistances are generated by using the end-resistance technique [10] as follows.

In the first measurement setup, a current $I_{g1}$ is forced to sweep through gate$_1$, while at the same time, both gate$_2$ and the drain are left open and the source is grounded. The voltage at gate$_1$ and the drain are measured simultaneously and given by

$$\frac{\Delta V_{g1}}{\Delta I_{g1}} = R_{g1} + \frac{n_1 V_T}{I_{g1}} + \frac{R_{c1}^f}{3} + R_s \tag{6}$$

$$\frac{V_d}{I_{g1}} = \frac{R_{c1}^f}{2} + R_s \tag{7}$$

where $R_{c1}^f$ is channel$_1$ resistance when gate$_1$ is forward biased. Equation (6) shows a straight line for $\Delta V_{g1}/\Delta I_{g1}$ versus $1/I_{g1}$ characteristics with $n_1 V_T$ as the slope and $R_{g1} + R_{c1}^f/3 + R_s$ as the intercept point.

The second measurement setup is similar to the first setup where a current $I_{g2}$ is forced to sweep through gate$_2$, while at the same time both gate$_1$ and the drain are left open and the source is grounded. The voltages at gate$_2$ and the drain are measured simultaneously. It can be shown that

$$\frac{\Delta V_{g2}}{\Delta I_{g2}} = R_{g2} + \frac{n_2 V_T}{I_{g2}} + \frac{R_{c2}^f}{3} + R_{12} + R_{c1} + R_s \tag{8}$$

$$\frac{V_d}{I_{g2}} = \frac{R_{c2}^f}{2} + R_{12} + R_{c1} + R_s \tag{9}$$

where $R_{c2}^f$ is channel$_2$ resistance when gate$_2$ is forward biased. Equation (8) shows a straight line for $\Delta V_{g2}/\Delta I_{g2}$ versus $1/I_{g2}$ characteristics with $n_2 V_T$ as the slope and $R_{g2} + R_{c2}^f/3 + R_{12} + R_{c1} + R_s$ as the intercept point.

In the third measurement setup, a current $I_{g1}$ is forced to sweep through gate$_1$, while a second current source sinks a current equal to gate$_1$ current, $I_{g1}$, out of the drain. At the same time, gate$_2$ is left open and the source is grounded. In this case, no current will flow to the source. The voltages at the drain is measured and given by

$$\frac{|V_d|}{I_{g1}} = \frac{R_{c1}^f}{2} + R_{12} + R_{c2} + R_d. \tag{10}$$

In the fourth measurement setup, a current $I_{g2}$ is forced to sweep through gate$_2$, while a second current source sinks a current equals to gate$_2$ current, $I_{g2}$, out of the drain. At the same time, gate$_1$ is left open and the source is grounded. No current will flow to the source. The voltages at both gate$_2$ and the drain are measured simultaneously. It can be shown that

$$\frac{\Delta(V_{g2} - V_d)}{\Delta I_{g2}} = R_{g2} + \frac{n_2 V_T}{I_{g2}} + \frac{R_{c2}^f}{3} + R_d \tag{11}$$

$$\frac{|V_d|}{I_{g2}} = \frac{R_{c2}^f}{2} + R_d. \tag{12}$$

Equation (11) shows a straight line for $\Delta(V_{g2} - V_d)/\Delta I_{g2} - (1/I_{g2})$ characteristics with $n_2 V_T$ as the slope and $R_{g2} + R_{c2}^f/3 + R_d$ as the intercept point.

In the fifth measurement setup, a current $I_{g1}$ is forced to sweep through gate$_1$, while a second current source sinks half of this current out of the drain. At the same time, gate$_2$ is left open and the source is grounded. The voltage at the drain is measured. In this case, the source current equals half of gate$_1$ current. Because $FET_1$ is driven symmetrically, no current will flow through $R_{c1}$ and the drain voltage is given by

$$\frac{2|V_d|}{I_{g1}} = R_{12} + R_{c2} + R_d - R_s. \tag{13}$$

The sixth measurement setup is similar to the fifth setup. In this setup, a current $I_{g2}$ is forced to sweep through gate$_2$, while a second current source sinks half of this current out of the drain. At the same time, gate$_1$ is left open and the source is grounded. The drain voltage is measured. Again, the source current $I_s$ equals half of gate$_2$ current. Because FET$_2$ is driven symmetrically, no current will flow through $R_{c2}$. The drain voltage can be written as

$$\frac{2V_d}{I_{g1}} = R_{12} + R_{c1} + R_s - R_d. \tag{14}$$

Equations (6)–(14) are used to extract all the nine unknown resistance values.

## III. Experimental Results

We applied this technique to characterize 29 1-$\mu$m dual-gate GaAs MESFETs with different topologies. These devices were fabricated at Nortel Networks, Ottawa, ON, Canada. For brevity, the extracted extrinsic resistances of only nine transistors are shown in Table I. The gate widths of these devices are: 1) $2 \times 50$ $\mu$m; 2) $2 \times 100$ $\mu$m; 3) $4 \times 25$ $\mu$m; 4) $4 \times 50$ $\mu$m; 5) $4 \times 100$ $\mu$m; 6) $6 \times 50$ $\mu$m, with the distance between gate$_1$ and the source ($L_{g1s}$) equal to 1.5 $\mu$m; 7) $6 \times 50$ $\mu$m, with $L_{g1s}$ equal to 3 $\mu$m; 8) $6 \times 50$ $\mu$m, with $L_{g1s}$ equal to 4.5 $\mu$m; and 9) $6 \times 50$ $\mu$m, with $L_{g1s}$ equal to 6 $\mu$m.

It can be seen that the scaling rules versus gate width are generally verified. The gate resistances scale to the number of gate fingers. This is similar to the results published in [7]. It is also clear that the source resistance, which includes bulk resistance of the region from the source to gate$_1$, increases with the distance $L_{g1s}$, as shown by the $6 \times 50$ $\mu$m devices (6)–(9).

It was found that if $R_c = R_c^f$ is assumed, the extracted source and drain resistances are under estimated. Since the channel resistance is smaller under forward bias condition, (7) and (12) show that the calculated source and drain resistances will be smaller than their real values. For example, if $R_c = R_c^f$ is assumed, the extracted resistances of device (6) are $R_s = 1.7\,\Omega$,

TABLE I
THE EXTRACTED EXTRINSIC RESISTANCES OF THE DGFET

| Device | $L_{g1s}$(μm) | $R_s$(Ω) | $R_{c1}$(Ω) | $R_{12}$(Ω) | $R_{c2}$(Ω) | $R_d$(Ω) | $R_{g1}$(Ω) | $R_{g2}$(Ω) |
|---|---|---|---|---|---|---|---|---|
| (1) 2x50 μm | 1.5 | 8.2 | 8 | 16 | 8 | 8.1 | 11.35 | 12.3 |
| (2) 2x100 μm | 1.5 | 4.2 | 4.1 | 8.2 | 4.1 | 4.1 | 11.25 | 12.2 |
| (3) 4x25 μm | 1.5 | 8 | 7.96 | 15.9 | 8 | 7.9 | 5.52 | 5.95 |
| (4) 4x50 μm | 1.5 | 4.2 | 4.23 | 8.5 | 4.28 | 4.16 | 5.4 | 5.87 |
| (5) 4x100 μm | 1.5 | 2.37 | 2.1 | 4.3 | 2.17 | 2.34 | 5.6 | 5.88 |
| (6) 6x50 μm | 1.5 | 2.87 | 2.8 | 5.6 | 2.82 | 2.8 | 3.57 | 3.9 |
| (7) 6x50 μm | 3 | 3.55 | 2.9 | 5.7 | 2.8 | 2.81 | 3.6 | 3.93 |
| (8) 6x50 μm | 4.5 | 4.2 | 2.9 | 5.54 | 2.8 | 2.78 | 3.56 | 3.94 |
| (9) 6x50 μm | 6 | 4.85 | 3 | 5.65 | 2.78 | 2.78 | 3.56 | 3.9 |

$R_{c1} = 3\,\Omega$, $R_{12} = 5.67\,\Omega$, $R_{c2} = 2.97\,\Omega$, $R_d = 1.64\,\Omega$, $R_{g1} = 3.96\,\Omega$, and $R_{g2} = 4.1\,\Omega$. In comparison with the values for of device (6) in Table I, the source and drain resistance values are affected more than the other parasitic resistances.

## IV. CONCLUSIONS

A simple technique to extract all the extrinsic resistances of the DGFET using dc measurements has been described. The technique has been tested on many DGFETs with different topologies. The results obtained showed that the described technique gives a practical and accurate approach to characterize the DGFET.

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